REMARKS

This is in full and timely response to the Office Action dated December 28, 2007.

Claims 45-50 are currently pending in this application, with claims 45 being independent. *No new matter has been added.*

Reexamination in light of the following remarks is respectfully requested.

Entry of amendment

This amendment *prima facie* places the case in condition for allowance. Alternatively, it places this case in better condition for appeal.

Accordingly, entry of this amendment is respectfully requested.

Prematureness

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office Action, respectfully requests reconsideration of the finality of the Final Office Action for the reasons set forth hereinbelow. See M.P.E.P. §706.07(c).

New non-final Office Action

At least for the following reasons, if the allowance of the claims is not forthcoming at the very least and a new ground of rejection made, then a ***new non-final Office Action*** is respectfully requested.

Rejection under 35 U.S.C. §112

Paragraph 6 of the Office Action indicates a rejection of claims 45-52 under 35 U.S.C. §112, second paragraph.

This rejection is traversed at least for the following reasons.

While not conceding the propriety of this rejection and in order to advance the prosecution of the above-identified application, claim 45 has been amended in the manner suggested by the Examiner.

Appreciation is expressed for this helpful suggestion.

Withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. §103

Paragraph 8 of the Office Action indicates a rejection of claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 to Sagane in view of U.S. Patent No. 5,784,537 to Suzuki et al. (Suzuki)

This rejection is traversed at least for the following reasons.

Claims 27-28 and 40 - While not conceding the propriety of this rejection and in order to advance the prosecution of the above-identified application, claims 27-28 and 40 have been canceled.

Withdrawal of this rejection is respectfully requested.

Paragraph 9 of the Office Action indicates a rejection of claims 27-28 and 40 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal) and in view U.S. Patent No. 5,784,537 (Suzuki).

Paragraph 10 of the Office Action indicates a rejection of claims 51 and 52 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,454,100 (Sagane) in view of U.S. Patent No. 6,412,081 (Koscal), and in view U.S. Patent No. 5,784,537 (Suzuki), and in further view U.S. Patent No. 5,701,506 (Hosotani).

This rejection is traversed at least for the following reasons.

Claim 51 has been wholly incorporated into claim 45. Since claim 51 has been examined within the Final Office Action, **no "*further search and/or consideration*" of amended claim 45 is believed to be required**.

Claim 45 is drawn to a data processing apparatus comprising:

> program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;
>
> a central processing unit adapted to process interrupt functions of different priority levels, one of said interrupt functions being processed upon receipt of a first interrupt request signal or a second interrupt request signal;
>
> a first coincidence detecting circuit adapted to compare said program address with a first bug address and output said first interrupt request signal, said central processing unit receiving said first interrupt request signal;
>
> a second coincidence detecting circuit adapted to compare said program address with a second bug address and output said second interrupt request signal, said central processing unit receiving said second interrupt request signal;

a counter register adapted to store a value, said value being incremented by 1 when said first interrupt request signal indicates a coincidence between said address and said first bug address or when said second interrupt request signal indicates a coincidence between said address and said second bug address,

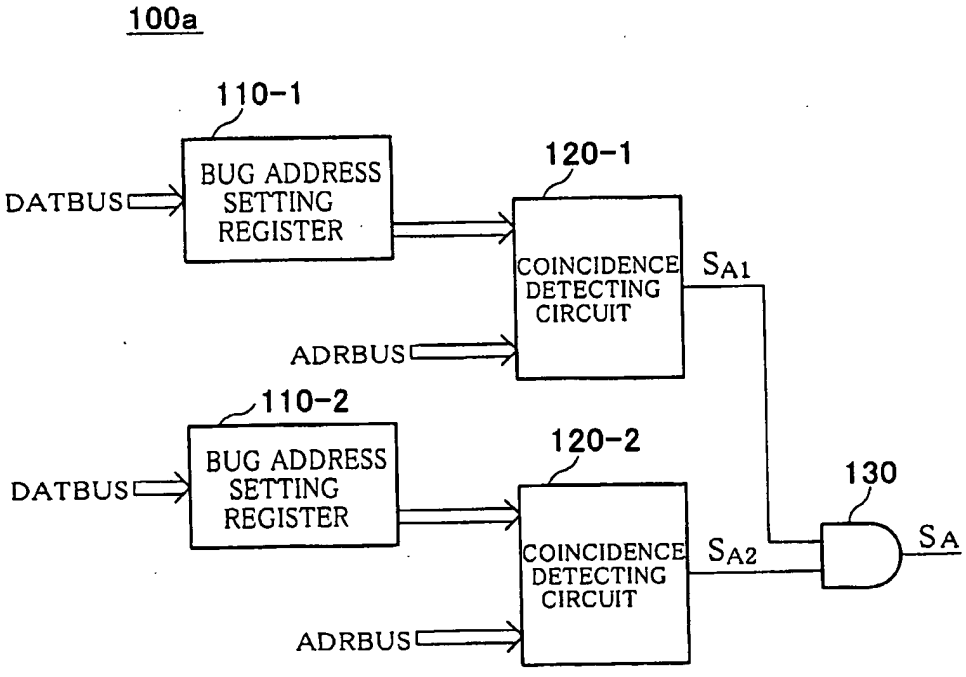
wherein said counter register is set to 0 during initialization processing,

wherein said first and second interrupt request signals are input to said central processing unit as a single interruption,

wherein said first and second interrupt request signals are AND'ed together to become said single interruption.

Figure 7 of the specification as originally filed is shown hereinbelow.

FIG.7



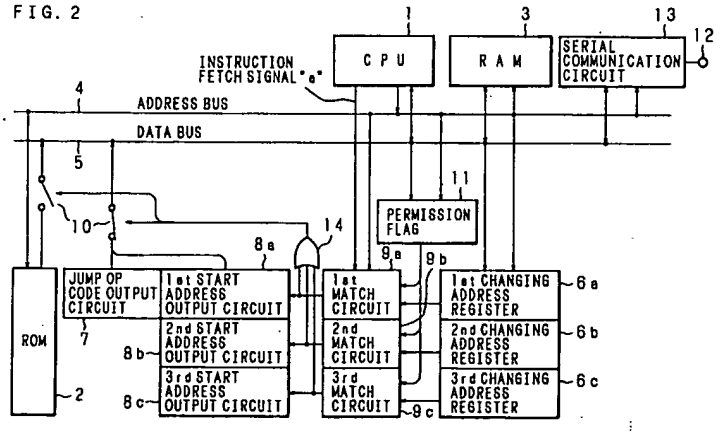
U.S. Patent Application Publication No. 2001/0052114, the publication document for the present application, provides in paragraph [0073] that:

> [0073] When there is sufficient leeway in the interrupt processing of the CPU 10, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 can be input to the CPU 10 as two different interrupt request signals. Accordingly, the CPU 10 receives these as different interrupt requests and executes the debugged programs separately to correct the two bugs. In general, however, the number of the interruptions that the CPU 10 is able to process is limited, so a plurality of bug processings have to be assigned to a single interruption. In this case, as shown in FIG. 7, the output signals SA1 and SA2 of the coincidence detecting circuits 120-1 and 120-2 are input to an AND gate 130, and the output signal S_A Of the AND gate 130 is input to the CPU 10 as the interrupt request signal.

Sagane, Koscal and Suzuki - The Office Action admits that Sagane, Koscal and Suzuki do not expressly disclose that wherein said first and second interrupt request signals are input to said central processing unit as a single interruption (Office Action at page 18).

Hosotani - The Office Action cites Hosotani for the features that are admittedly absent from within Sagane, Koscal and Suzuki. Figure 2 of Hosotani is shown hereinbelow.

FIG. 2



Hosotani arguably teaches that *the CPU 1* is also connected, via the address bus 4 and a signal line of an instruction fetch signal a, to the *first to third match circuits 9a to 9c* that respectively compare the change addresses with the address on the address bus 4 in synchronism with the output timing of the instruction fetch signal a from *the CPU 1*, and output signals indicating the results of the comparisons (a "1" level indicates an address match, and a "0" level indicates an address mismatch) (Hosotani at column 4, lines 46-53).

However, Hosotani fails to disclose, teach, or suggest the signals from the first to third match circuits 9a-9c being input to CPU 1.

The first to third match circuits 9a-9c are connected to a three-input OR circuit 14 (Hosotani at column 4, lines 60-61).

However, Hosotani fails to disclose, teach, or suggest the signals from the three-input OR circuit 14 being input to CPU 1.

Instead, *the output of the OR circuit 14 is **connected to a connection control means 10*** which selects either the mask ROM 2 or a jump op code output circuit 7 and first to third start address output circuits 8a-8c for connection to the data bus 5 in accordance with the output level of the OR circuit 14 (which outputs a "1" level when the result of comparison from any one of the match circuits 9a-9c indicates a match, and a "0" level when all the comparison results indicate a mismatch) (Hosotani at column 4, line 61, to column 5, line 2).

- ***Thus, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are input to said central processing unit as a single interruption.***

- ***Moreover, Hosotani fails to disclose, teach, or suggest a data processing apparatus wherein said first and second interrupt request signals are AND'ed together to become said single interruption.***

Withdrawal of this rejection is respectfully requested.

Conclusion

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Therefore, this response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

There is no concession as to the veracity of Official Notice, if taken in any Office Action. An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees. If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: February 15, 2008

Respectfully submitted,

By 40,290

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